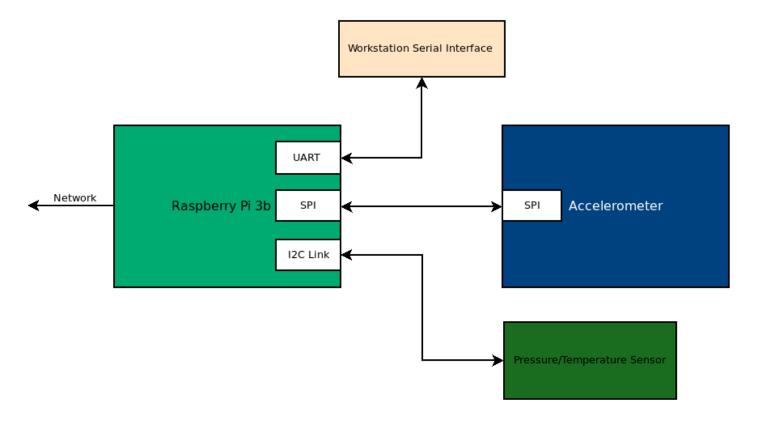


E210 Engineering Cyber-Physical Systems

Serial Peripheral Interface (SPI)

Weekly Focus	Reading	Monday	Wed	Lab
CPS Intro/UART		1/10: CPS Introduction	1/12: Pi Intro/UART Bus	Project 0 Raspberry PI Setup
I2C Bus		1/17: MLK Day	1/19: I2C Bus Overview	Project 1 I2C Pressure/Temperature Sensor
I2C and SPI Bus		1/24: Pressure Sensor	1/26: SPI Bus Overview	Project 2 SPI Accelerometer
SPI/Networking		1/31: Accelerometer	2/2: Networking Overview Project 3 Flask Web Server	
Networking		2/7: Flask	2/9: Redis/matplotlib	Project 3 Continued
Web Server		2/14: CPS Wrapup	2/16: Exam Review	P5 Demultiplexer

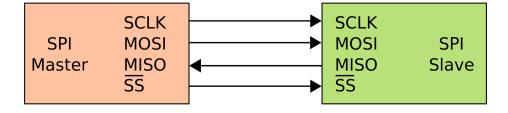
Raspberry SPI Link



SPI Overview

What is SPI?

- 1. Synchronous Serial Link
- 2. 4 Wire Bus



- 3. Devices Selected with Chip Select Pin
- 4. Full Duplex
- 5. Only One Bus Controller



History of SPI

- Developed by Motorola in mid-80s
- Short distance communication for embedded systems
- ystems

- De facto standard
- Significantly faster than I2C or UART communication
 - Max Speeds Typically 20Mbps+ (no minimum speed)
- Used in SD Cards and Embedded LCD displays

Category	SPI	I2C	UART
Clock	Synchronous	Synchronous	Asynchronous
Speed	20 Mbps +	400K Baud (5M Baud Max)	115K Baud
Transmission Mode	Full Duplex	Half Duplex	Full Duplex
Number of Devices	Only Limited by CS Pins	112 (1024 possible)	2
Number of Pins	3 + CS	2 (Data, Clock)	2* (Rx, Tx), Optional (CTS,RTS)
Baud Rate Accuracy Requirement	N/A	N/A	~3% Baud Rate Accuracy
Development Complexity	Low	Med	Low

Device Naming Conventions

Open Source Hardware Association

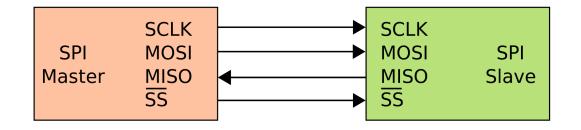
New Name	Old Name
SDO – Serial Data Out	MOSI – Master Out Slave In
SDI – Serial Data In	MISO – Master In Slave Out
CS – Chip Select	SS – Slave Select
SCLK - Clock	SCLK - Clock

https://www.oshwa.org/a-resolution-to-redefine-spi-signal-names

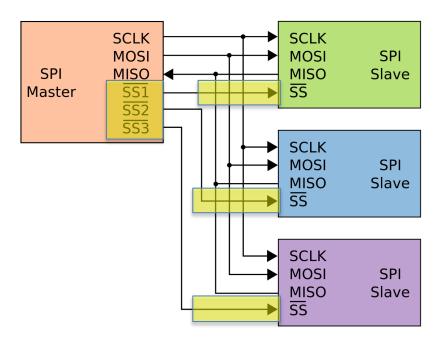


Bus Connections

Single Peripheral



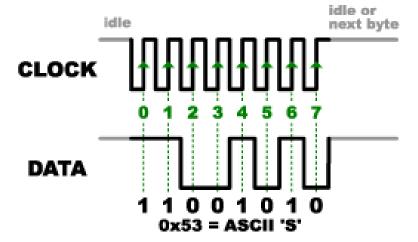
Multiple Independent Peripherals



Bus Protocol

Sending Data

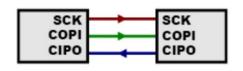


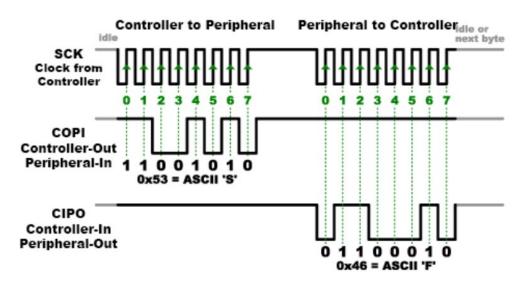


https://learn.sparkfun.com/tutorials/serial-peripheral-interface-spi/all



Receiving Data

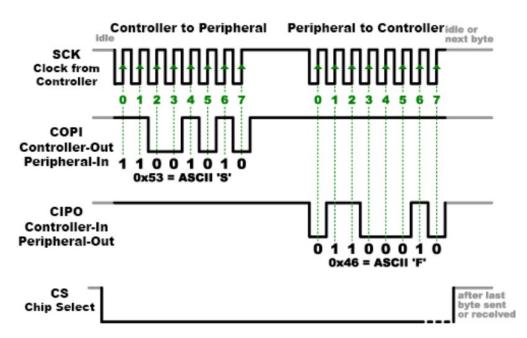




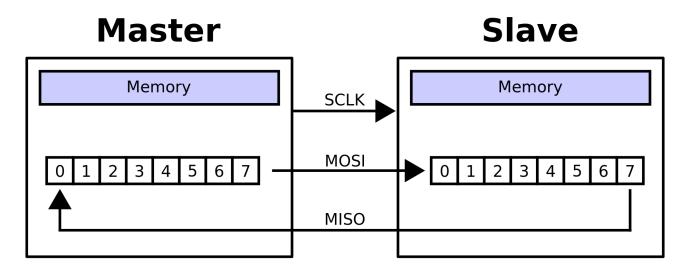
https://learn.sparkfun.com/tutorials/serial-peripheral-interface-spi/all

Chip Select





16-bit Shift Register (split between two chips)



Swaps Registers

Waveform

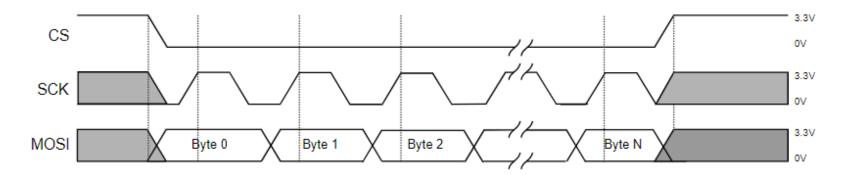
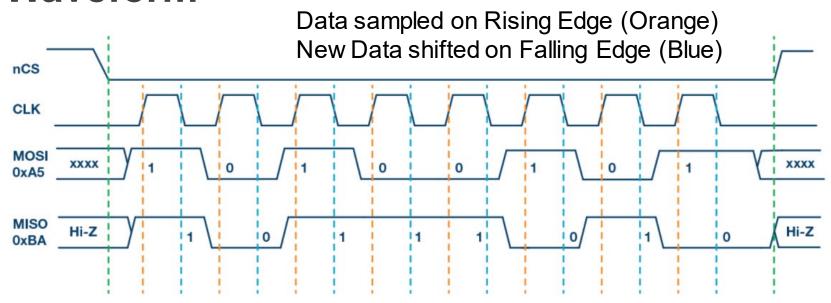


Figure + Frample of a SPI transmission

Waveform



```
* Simultaneously transmit and receive a byte on the SPI.
 * Polarity and phase are assumed to be both 0, i.e.:
   - input data is captured on rising edge of SCLK.
     - output data is propagated on falling edge of SCLK.
 * Returns the received byte.
uint8 t SPI transfer byte(uint8 t byte out)
   uint8 t byte in = 0;
   uint8 t bit;
   for (bit = 0x80; bit; bit >>= 1) {
       /* Shift-out a bit to the MOSI line */
       write MOSI((byte out & bit) ? HIGH : LOW);
       /* Delay for at least the peer's setup time */
       delay(SPI_SCLK_LOW_TIME);
       /* Pull the clock line high */
       write SCLK(HIGH);
       /* Shift-in a bit from the MISO line */
       if (read MISO() == HIGH)
           byte in |= bit;
       /* Delay for at least the peer's hold time */
       delay(SPI SCLK HIGH TIME);
       /* Pull the clock line low */
       write SCLK(LOW);
   return byte in;
```

```
* Simultaneously transmit and receive a byte on the SPI.
 * Polarity and phase are assumed to be both 0, i.e.:
    - input data is captured on rising edge of SCLK.
     - output data is propagated on falling edge of SCLK.
 * Returns the received byte.
uint8 t SPI transfer byte(uint8 t byte out)
   uint8 t byte in = 0;
   uint8 t bit;
    for (bit = 0x80; bit; bit >>= 1) {
       /* Shift-out a bit to the MOSI line */
        write_MOSI((byte_out & bit) ? HIGH : LOW);
        /* Delay for at least the peer's setup time */
        delay(SPI_SCLK_LOW_TIME);
        /* Pull the clock line high */
        write SCLK(HIGH);
        /* Shift-in a bit from the MISO line */
        if (read MISO() == HIGH)
            byte in |= bit;
        /* Delay for at least the peer's hold time */
        delay(SPI SCLK HIGH TIME);
        /* Pull the clock line low */
        write SCLK(LOW);
    return byte in;
```

```
* Simultaneously transmit and receive a byte on the SPI.
 * Polarity and phase are assumed to be both 0, i.e.:
    - input data is captured on rising edge of SCLK.
     - output data is propagated on falling edge of SCLK.
 * Returns the received byte.
uint8 t SPI transfer byte(uint8 t byte out)
   uint8 t byte in = 0;
   uint8 t bit;
    for (bit = 0x80; bit; bit >>= 1) {
        /* Shift-out a hit to the MOST line */
        write MOSI((byte out & bit) ? HIGH : LOW);
        /* Delay for at least the peer's setup time */
        delay(SPI_SCLK_LOW_TIME);
        /* Pull the clock line high */
        write SCLK(HIGH);
        /* Shift-in a bit from the MISO line */
        if (read MISO() == HIGH)
            byte in |= bit;
        /* Delay for at least the peer's hold time */
        delay(SPI SCLK HIGH TIME);
        /* Pull the clock line low */
        write SCLK(LOW);
    return byte in;
```

```
* Simultaneously transmit and receive a byte on the SPI.
 * Polarity and phase are assumed to be both 0, i.e.:
   - input data is captured on rising edge of SCLK.
     - output data is propagated on falling edge of SCLK.
 * Returns the received byte.
uint8 t SPI transfer byte(uint8 t byte out)
   uint8 t byte in = 0;
   uint8 t bit;
   for (bit = 0x80; bit; bit >>= 1) {
       /* Shift-out a bit to the MOSI line */
       write MOSI((byte out & bit) ? HIGH : LOW);
        /* Delay for at least the peer's setup time */
       delay(SPI SCLK LOW TIME);
       /* Pull the clock line high */
       write SCLK(HIGH);
       /* Shift-in a bit from the MISO line */
       if (read MISO() == HIGH)
           byte in |= bit;
       /* Delay for at least the peer's hold time */
       delay(SPI SCLK HIGH TIME);
       /* Pull the clock line low */
       write SCLK(LOW);
   return byte in;
```

```
* Simultaneously transmit and receive a byte on the SPI.
 * Polarity and phase are assumed to be both 0, i.e.:
    - input data is captured on rising edge of SCLK.
     - output data is propagated on falling edge of SCLK.
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       write MOSI((byte out & bit) ? HIGH : LOW);
       /* Delay for at least the peer's setup time */
       delay(SPI_SCLK_LOW_TIME);
        /* Pull the clock line high */
       write SCLK(HIGH);
       /* Shift-in a bit from the MISO line */
       if (read MISO() == HIGH)
           byte in |= bit;
       /* Delay for at least the peer's hold time */
       delay(SPI SCLK HIGH TIME);
       /* Pull the clock line low */
       write SCLK(LOW);
   return byte in;
```

```
* Simultaneously transmit and receive a byte on the SPI.
 * Polarity and phase are assumed to be both 0, i.e.:
    - input data is captured on rising edge of SCLK.
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        write MOSI((byte out & bit) ? HIGH : LOW);
        /* Delay for at least the peer's setup time */
        delay(SPI_SCLK_LOW_TIME);
        /* Pull the clock line high */
        write SCLK(HIGH);
        /* Shift-in a bit from the MISO line */
        if (read MISO() == HIGH)
            byte in |= bit;
        /* Delay for at least the peer's hold time */
        delay(SPI SCLK HIGH TIME);
        /* Pull the clock line low */
        write SCLK(LOW);
    return byte in;
```

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* Simultaneously transmit and receive a byte on the SPI.
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        write MOSI((byte out & bit) ? HIGH : LOW);
        /* Delay for at least the peer's setup time */
        delay(SPI_SCLK_LOW_TIME);
        /* Pull the clock line high */
        write SCLK(HIGH);
        /* Shift-in a bit from the MISO line */
        if (read MISO() == HIGH)
           byte in |= bit;
        /* Delay for at least the peer's hold time */
        delay(SPI SCLK HIGH TIME);
        /* Pull the clock line low */
        write SCLK(LOW);
    return byte in;
```

```
* Simultaneously transmit and receive a byte on the SPI.
 * Polarity and phase are assumed to be both 0, i.e.:
   - input data is captured on rising edge of SCLK.
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       /* Shift-out a bit to the MOSI line */
       write MOSI((byte out & bit) ? HIGH : LOW);
       /* Delay for at least the peer's setup time */
       delay(SPI_SCLK_LOW_TIME);
       /* Pull the clock line high */
       write SCLK(HIGH);
       /* Shift-in a bit from the MISO line */
       if (read MISO() == HIGH)
           byte in |= bit;
       /* Delay for at least the peer's hold time */
       delay(SPI SCLK HIGH TIME);
        /* Pull the clock line low */
       write SCLK(LOW);
   return byte in;
```

Register Addressing

Reading

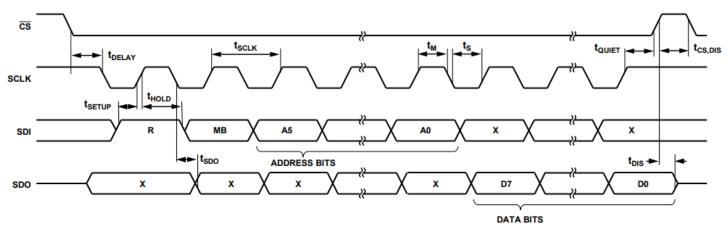
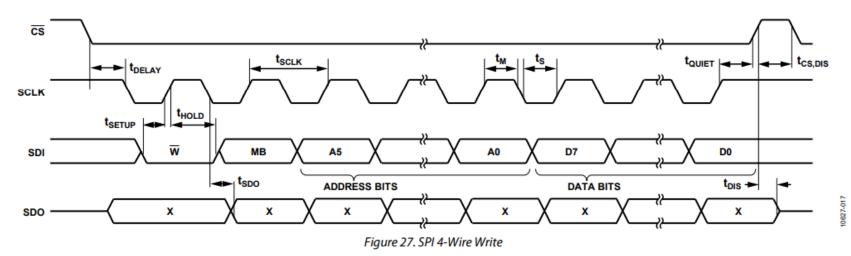
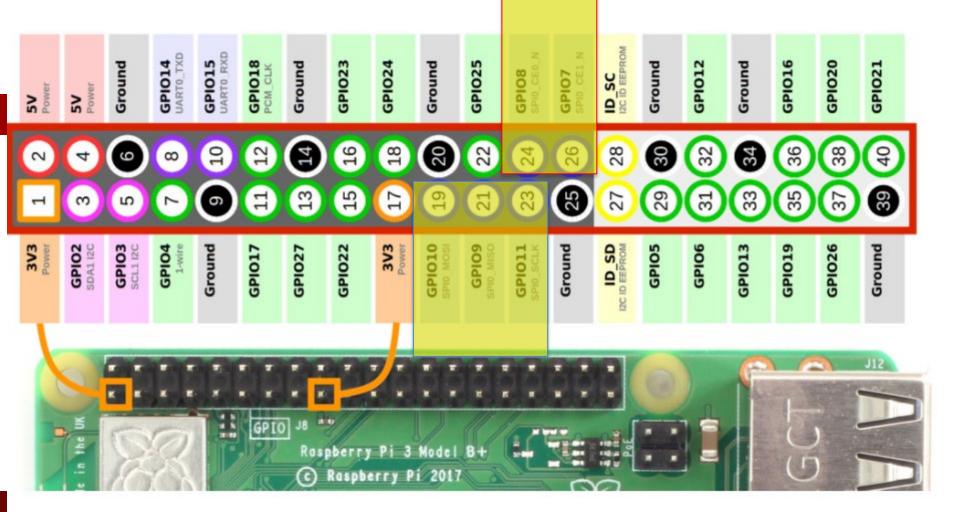


Figure 28. SPI 4-Wire Read

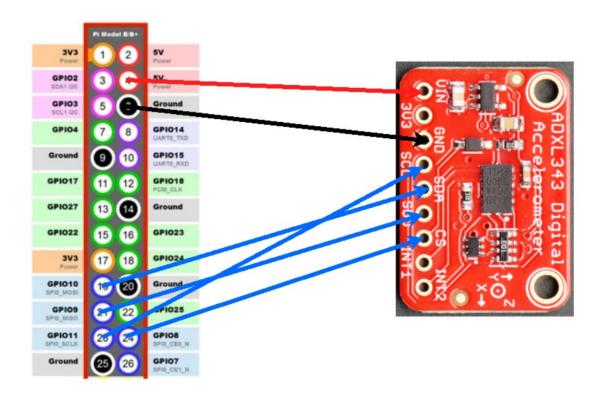
Writing



Raspberry Pi Python SPI



ADXL343 Accelerometer





3-Axis, ± 2 g/ ± 4 g/ ± 8 g/ ± 16 g Digital MEMS Accelerometer

Data Sheet ADXL343

FEATURES

Multipurpose accelerometer with 10- to 13-bit resolution for use in a wide variety of applications

Digital output accessible via SPI (3- and 4-wire) and I²C Built-in motion detection features make tap, double-tap, activity, inactivity, and free-fall detection trivial User-adjustable thresholds

Interrupts independently mappable to two interrupt pins Low power operation down to 23 µA and embedded FIFO for reducing overall system power

Wide supply voltage range: 2.0 V to 3.6 V I/O voltage 1.7 V to V₅

Wide operating temperature range (-40°C to +85°C) 10.000 a shock survival

Small, thin, Pb free, RoHS compliant 3 mm \times 5 mm \times 1 mm LGA package

APPLICATIONS

Handsets
Gaming and pointing devices
Hard disk drive (HDD) protection

GENERAL DESCRIPTION

The ADXL343 is a versatile 3-axis, digital-output, low g MEMS accelerometer. Selectable measurement range and bandwidth, and configurable, built-in motion detection make it suitable for sensing acceleration in a wide variety of applications. Robustness to 10,000 g of shock and a wide temperature range (-40°C to +85°C) enable use of the accelerometer even in harsh environments.

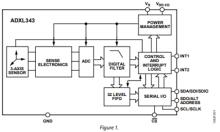
The ANXI.343 measures acceleration with high resolution (13-bit) measurement at up to ±16 g. Digital output data is formatted as 16-bit twos complement and is accessible through either an SPI (3-or 4-wire) or PC digital interface. The ANXI.343 can measure the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (3.9 mg/ISB) enables measurement of inclination changes less than 1.0°.

Several special sensing functions are provided. Activity and inactivity sensing detect the presence or lack of motion. Tap sensing detects single and double taps in any direction. Free-fall sensing detects if the device is falling. These functions can be mapped individually to either of two interrupt output pins.

An integrated memory management system with a 32-level first in, first out (FIFO) buffer can be used to store data to minimize host processor activity and lower overall system power consumption.

The ADXL343 is supplied in a small, thin, $3~\text{mm} \times 5~\text{mm} \times 1~\text{mm}$, 14-terminal, plastic package.

FUNCTIONAL BLOCK DIAGRAM



ADXL343 Data Sheet

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Voovo	Digital Interface Supply Voltage.
2	GND	This pin must be connected to ground.
3	RESERVED	Reserved. This pin must be connected to Vs or left open.
4	GND	This pin must be connected to ground.
5	GND	This pin must be connected to ground.
6	Vs	Supply Voltage.
7	CS	Chip Select.
8	INT1	Interrupt 1 Output.
9	INT2	Interrupt 2 Output.
10	NC	Not Internally Connected.
11	RESERVED	Reserved. This pin must be connected to ground or left open.
12	SDO/ALT ADDRESS	Serial Data Output (SPI 4-Wire)/Alternate I ² C Address Select (I ² C).
13	SDA/SDI/SDIO	Serial Data (I ² C)/Serial Data Input (SPI 4-Wire)/Serial Data Input and Output (SPI 3-Wire).
14	SCL/SCLK	Serial Communications Clock. SCL is the clock for I ² C, and SCLK is the clock for SPI.

```
import spidev
import time
import numpy as np
class adx1343:
    def init (self,spi device=0, ce pin=0, speed=1000000):
        self.spi = spidev.SpiDev()
        self.spi.open(spi device, ce pin)
        self.spi.max speed hz = speed # Sets the maximum speed of the SPI link
        self.spi.mode = 0b11
        time.sleep(0.5)
        if self.get_device_id() == '0xe5':
           self.enable()
            print("Device ID Incorrect")
```

spidev Documentation

1. https://pypi.org/project/spidev/

Max Clock Speed

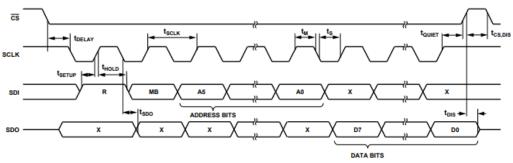
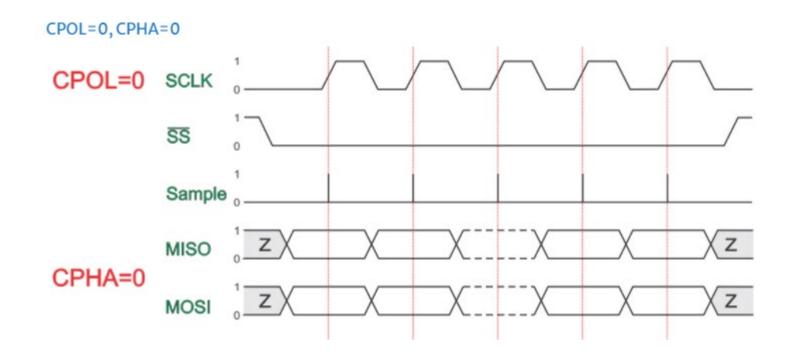


Figure 28. SPI 4-Wire Read

Table 10. SPI Timing $(T_A = 25^{\circ}C, V_S = 2.5 \text{ V}, V_{DD \text{ I/O}} = 1.8 \text{ V})^{1}$

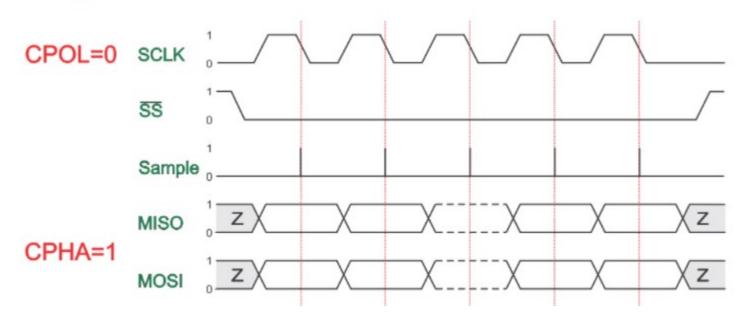
	Limit ^{2, 3}			
Parameter	Min	Max	Unit	Description
f _{SCLK}		5	MHz	SPI clock frequency
t _{SCLK}	200		ns	1/(SPI clock frequency) mark-space ratio for the SCLK input is 40/60 to 60/40
TDELAY	5		ns	CS falling edge to SCLK falling edge
t _{QUIET}	5		ns	SCLK rising edge to CS rising edge
tos		10	ns	CS rising edge to SDO disabled
t _{CS,DIS}	150		ns	CS deassertion between SPI communications
ts	$0.3 \times t_{SCLK}$		ns	SCLK low pulse width (space)
t _M	$0.3 \times t_{SCLK}$		ns	SCLK high pulse width (mark)
t setup	5		ns	SDI valid before SCLK rising edge
t HOLD	5		ns	SDI valid after SCLK rising edge
t _{spo}		40	ns	SCLK falling edge to SDO/SDIO output transition
t _R ⁴		20	ns	SDO/SDIO output high to output low transition
t _F ⁴		20	ns	SDO/SDIO output low to output high transition

SPI Polarity and Phase (mode=0b00)



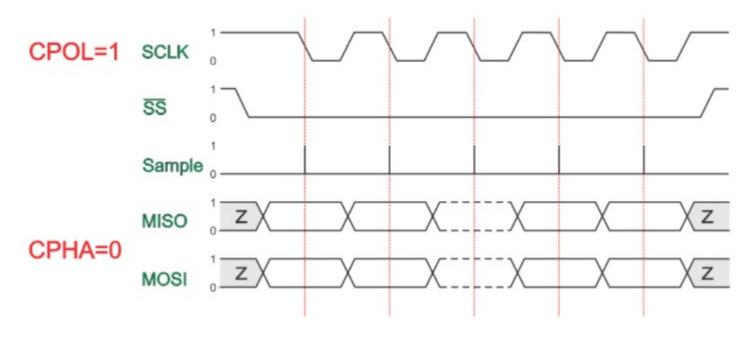
SPI Polarity and Phase (mode=0b01)

CPOL=0, CPHA=1



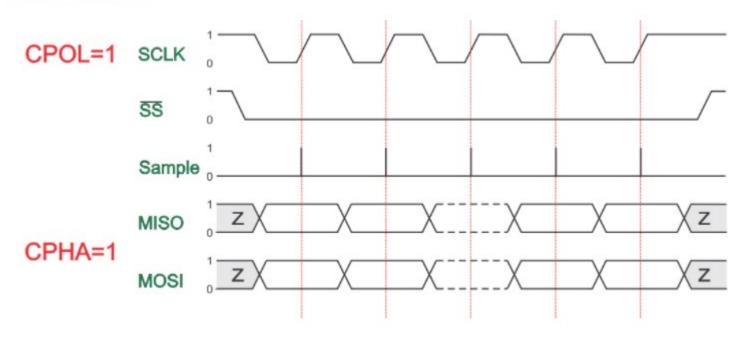
SPI Polarity and Phase (mode=0b10))

CPOL=1, CPHA=0



SPI Polarity and Phase (mode=0b11)

CPOL=1, CPHA=1



What the polarity and phase of this waveform?

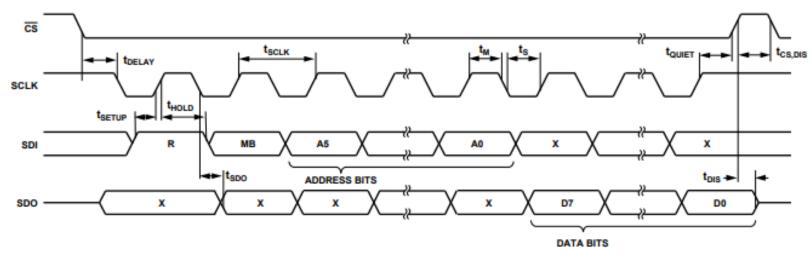


Figure 28. SPI 4-Wire Read

Registers

REGISTER MAP

Table 19.

Address					
Hex	Dec	Name	Туре	Reset Value	Description
0x00	0	DEVID	R	11100101	Device ID
0x01 to 0x1C	1 to 28	Reserved			Reserved; do not access
0x1D	29	THRESH_TAP	R/W	00000000	Tap threshold
0x1E	30	OFSX	R/W	00000000	X-axis offset
0x1F	31	OFSY	R/W	00000000	Y-axis offset
0x20	32	OFSZ	R/W	00000000	Z-axis offset
0x21	33	DUR	R/W	00000000	Tap duration
0x22	34	Latent	R/W	00000000	Tap latency
0x23	35	Window	R/W	00000000	Tap window
0x24	36	THRESH_ACT	R/W	00000000	Activity threshold
0x25	37	THRESH_INACT	R/W	00000000	Inactivity threshold
0x26	38	TIME_INACT	R/W	00000000	Inactivity time
0x27	39	ACT_INACT_CTL	R/W	00000000	Axis enable control for activity and inactivity detection
0x28	40	THRESH_FF	R/W	00000000	Free-fall threshold
0x29	41	TIME_FF	R/W	00000000	Free-fall time
0x2A	42	TAP_AXES	R/W	00000000	Axis control for single tap/double tap
0x2B	43	ACT_TAP_STATUS	R	00000000	Source of single tap/double tap
0x2C	44	BW_RATE	R/W	00001010	Data rate and power mode control
0x2D	45	POWER_CTL	R/W	00000000	Power-saving features control
0x2E	46	INT_ENABLE	R/W	00000000	Interrupt enable control
0x2F	47	INT_MAP	R/W	00000000	Interrupt mapping control
0x30	48	INT_SOURCE	R	00000010	Source of interrupts
0x31	49	DATA_FORMAT	R/W	00000000	Data format control
0x32	50	DATAX0	R	00000000	X-Axis Data 0
0x33	51	DATAX1	R	00000000	X-Axis Data 1
0x34	52	DATAY0	R	00000000	Y-Axis Data 0
0x35	53	DATAY1	R	00000000	Y-Axis Data 1
0x36	54	DATAZO	R	00000000	Z-Axis Data 0
0x37	55	DATAZ1	R R/W	00000000	Z-Axis Data 1
0x38	56	FIFO_CTL		00000000	FIFO control
0x39	57	FIFO_STATUS	R	00000000	FIFO status

Write Register

```
def write_register(self, address, data):
        self.spi.xfer2([address,data])
        return(0)
```

Read Register

```
def read register(self, address):
        address = address \mid 0x80
        read bytes = self.spi.xfer2([address,0x00])
        return (read bytes[1])
```