ENGR 210 / CSCI B441
“Digital Design”

SPI II

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Announcements

- P8 – Elevator Controller is out
  - This one is hard.

due Friday

- P9 – SPI is out → Last one

  - This one is new. Might be some changes.

- The end is in sight…

P9 SPI QuickStart

- We build the Vivado project for you:

```
git clone https://github.com/ENGR210/P9_SPI.git
cd P9_SPI
make setup
vivado vivado/vivado.xpr
```

- We provide you with Testbenches

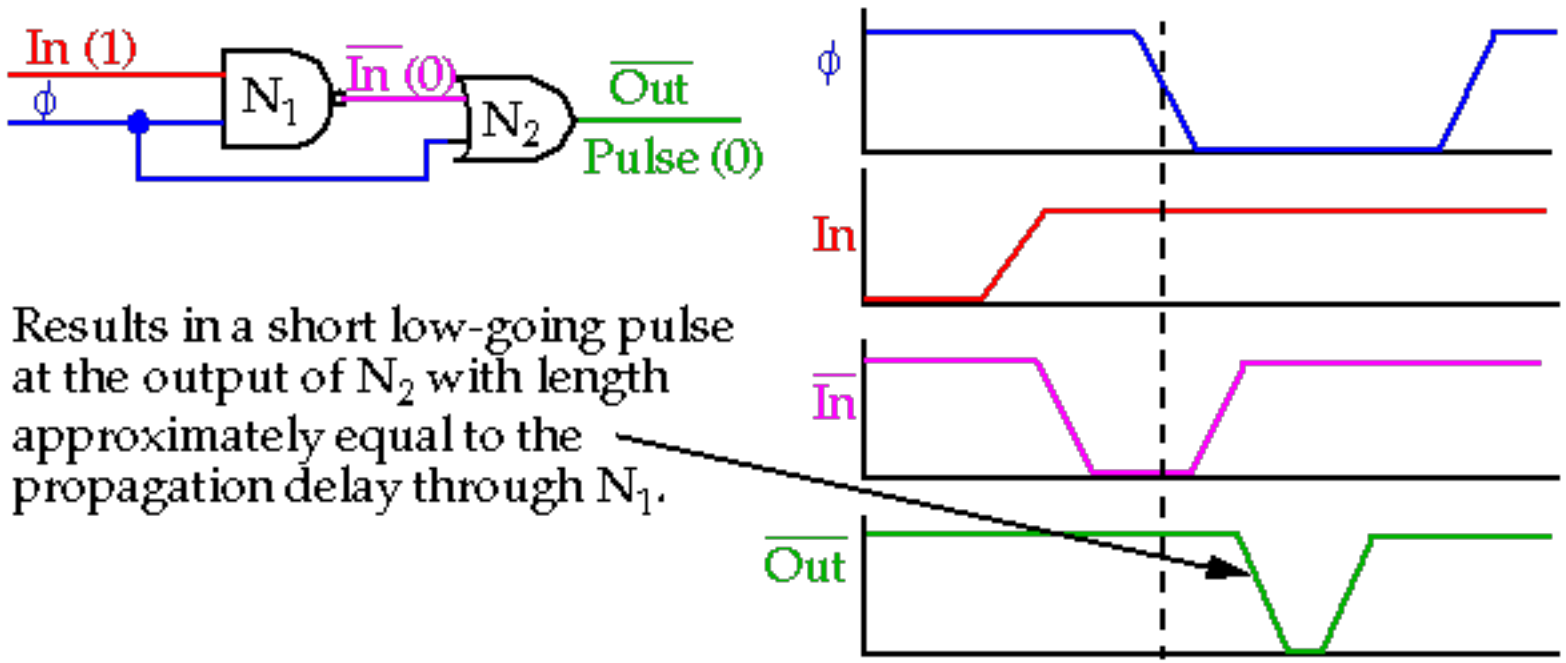
- Same ones as the Autograder!

Always specify defaults for `always_comb`!

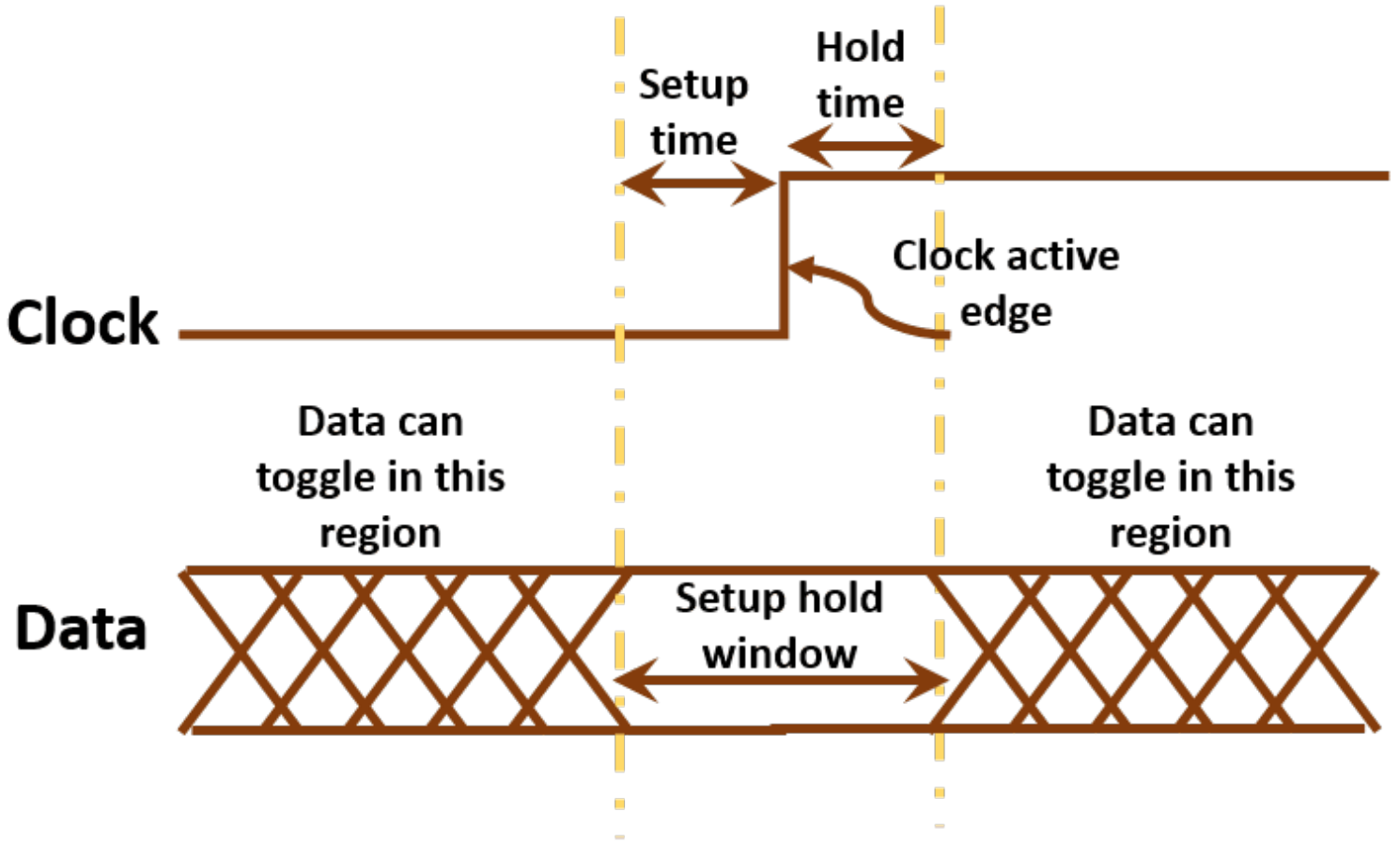
BLOCKING (=) FOR `always_comb`

NON-BLOCKING (<=) for `always_ff`

Glitch


In (1)
ϕ
N1
In (0)
N2
Out
Pulse (0)
ϕ
In
In
Out
Results in a short low-going pulse at the output of N2 with length approximately equal to the propagation delay through N1.

Setup/Hold Time



Slack

- Extra time between combinational propagation delay and setup time
- Time between stable input to Flip-Flop and next clock edge

- Vivado:
  - WNS: Worst-case Negative Slack

- If this number is <0, your circuit will (probably) not work

Correct `for(;;)` Loops in Verilog

This Code:

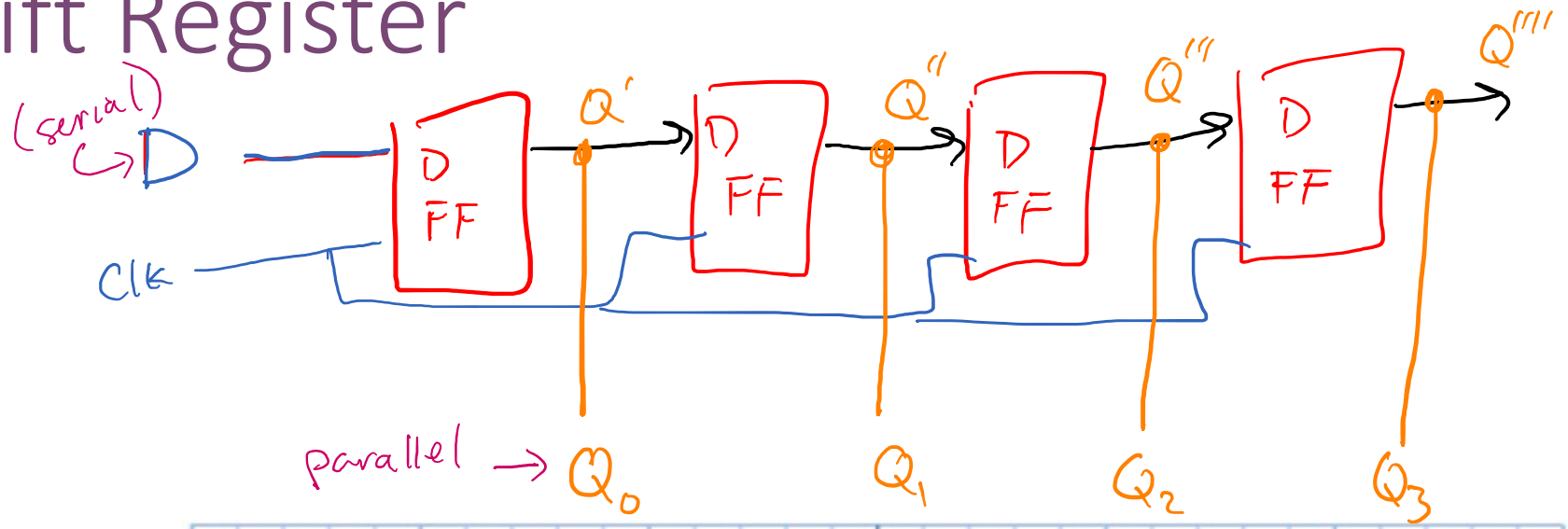
```
integer x; //or genvar x
for (x = 0; x < 4; x++) begin
     assign y[x] = a[x+right];
end
```

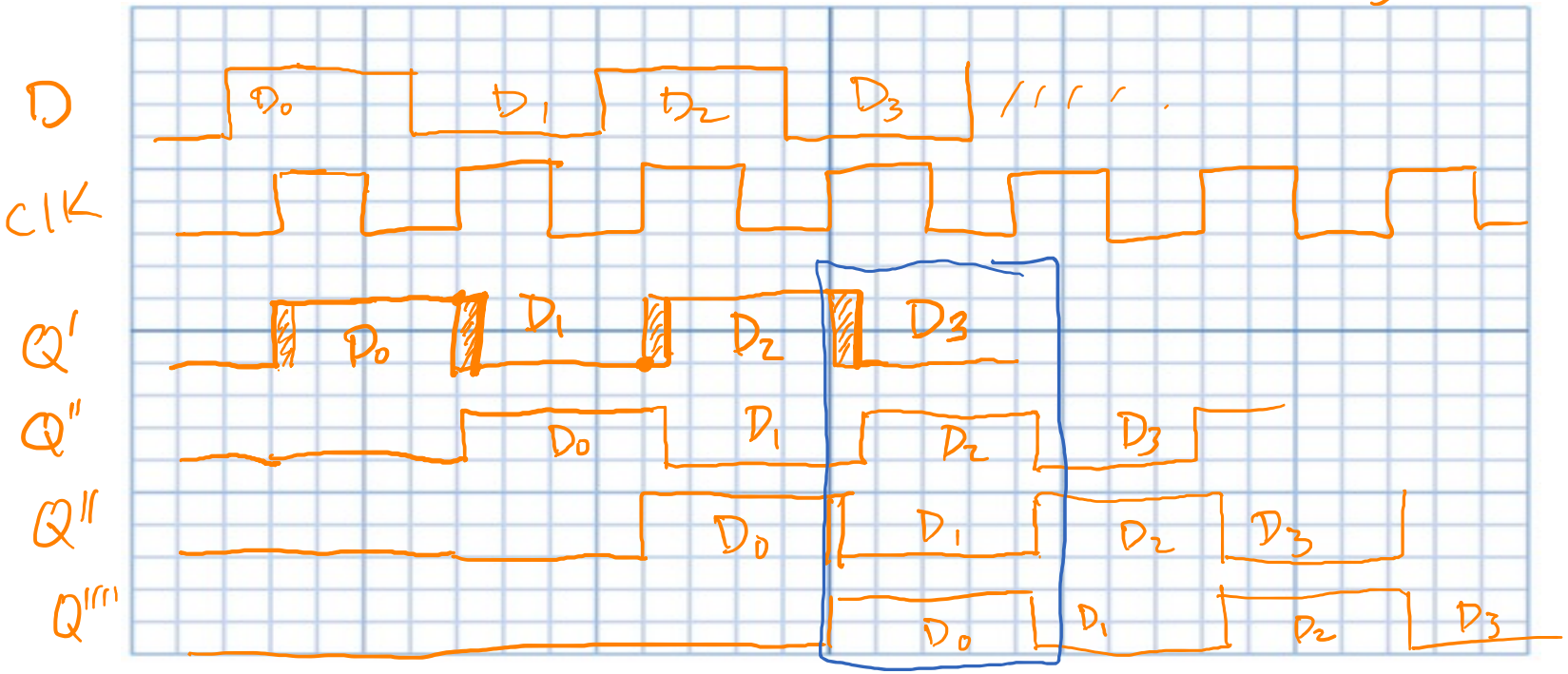
Expands to:

```
assign y[0] = a[0 + right];
assign y[1] = a[1 + right];
assign y[2] = a[2 + right];
assign y[3] = a[3 + right];
```

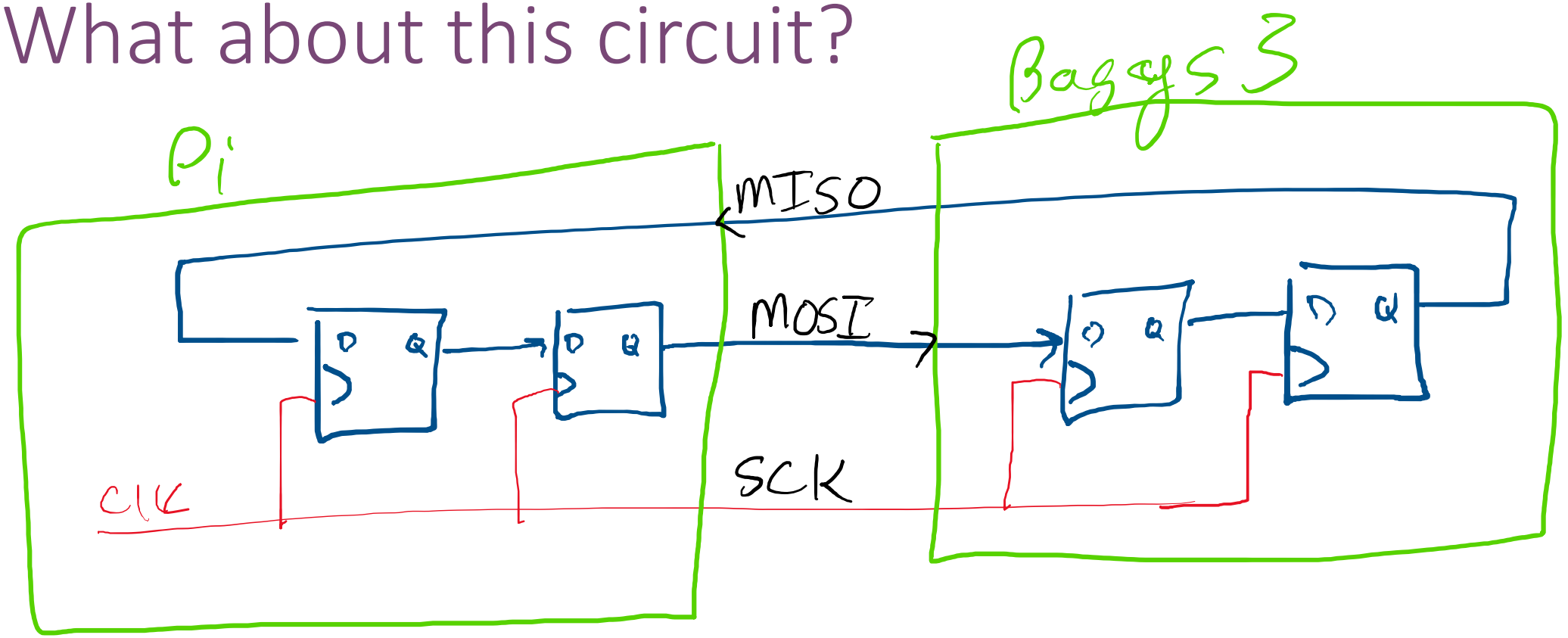
Converts serial input to parallel output

Shift Register





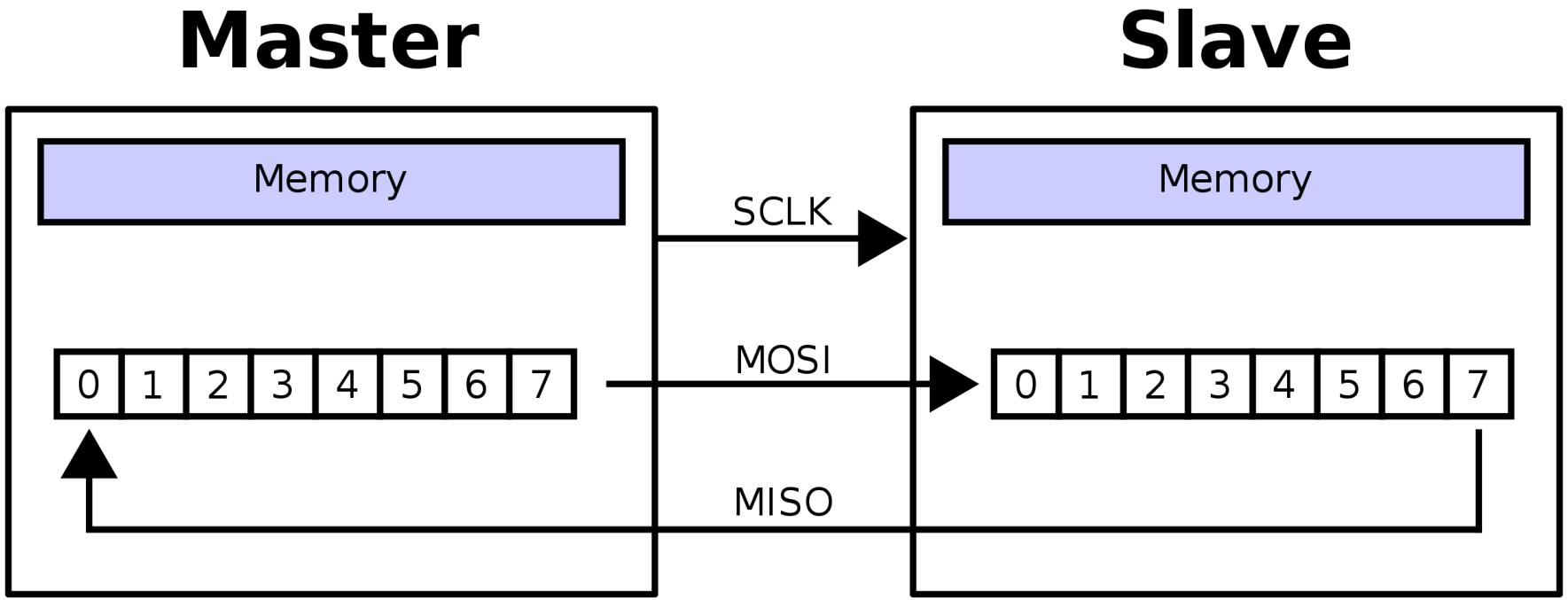
What about this circuit?



MOSI: Master Out Slave In
Serial Data Out (SDO)

MISO: Master In Slave Out
Serial Data In (SDI)

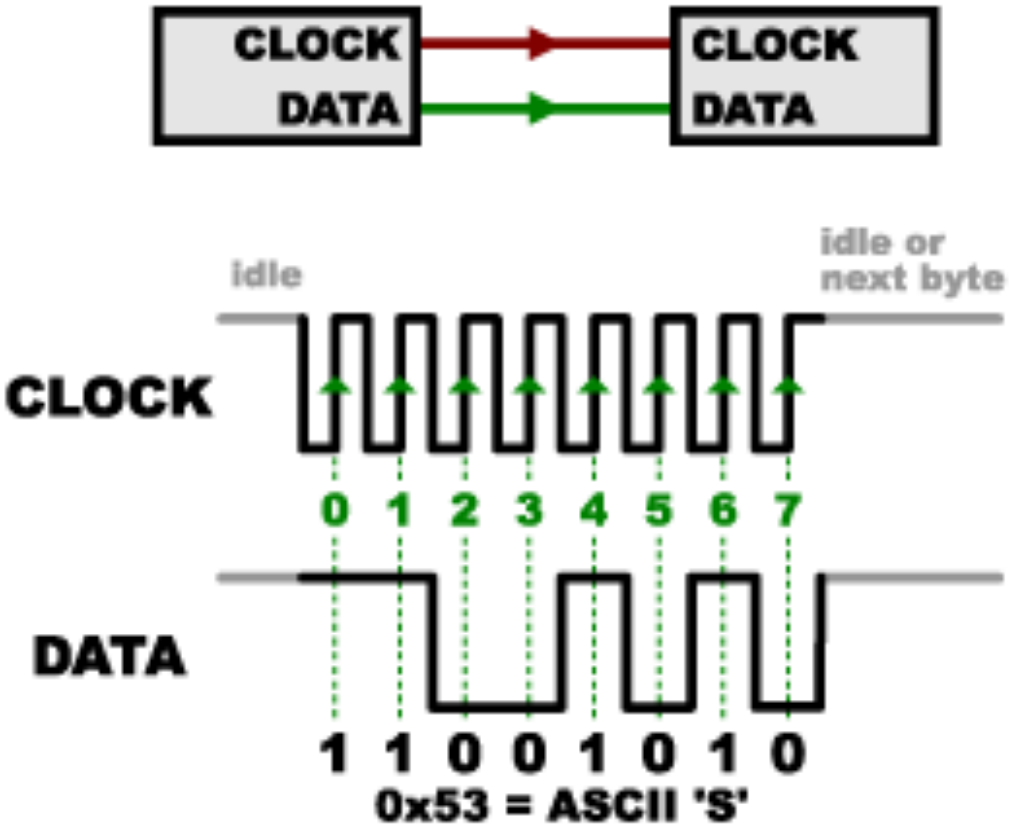
SPI


Master
Slave
Memory
Memory
SCLK
MOSI
MISO
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7

[wiki]

When to CAPTURE new data?

Rising Edge of SCK!

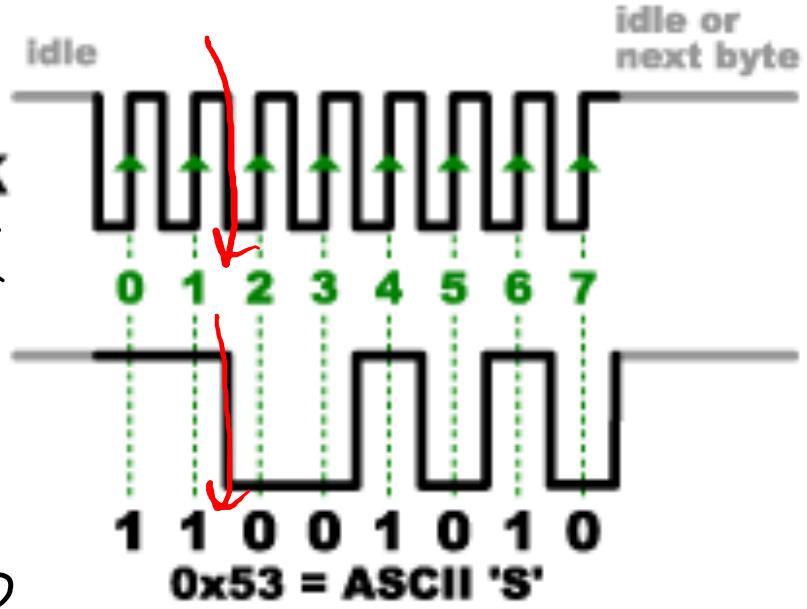


When to SEND new data?

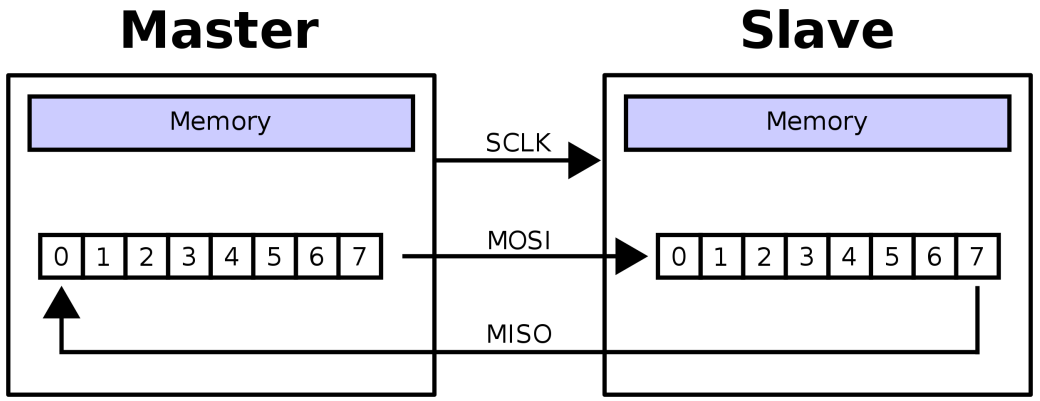
@ falling edge of SCK

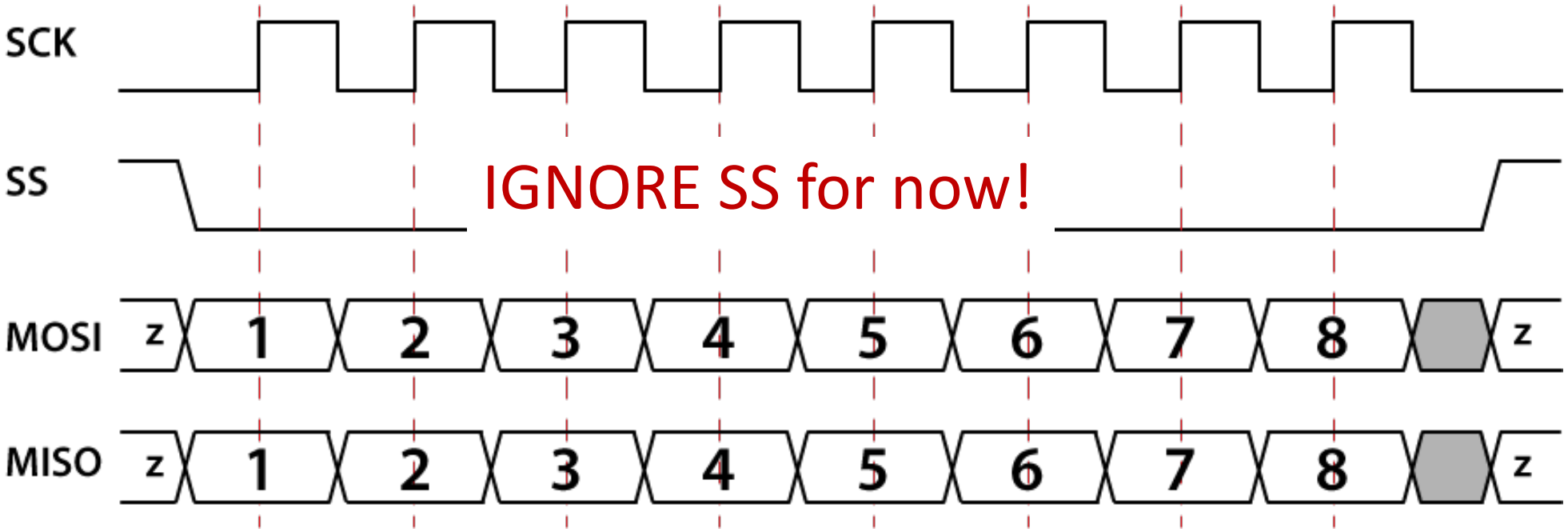
~~CLOCK~~ SCK

~~DATA~~ MISO



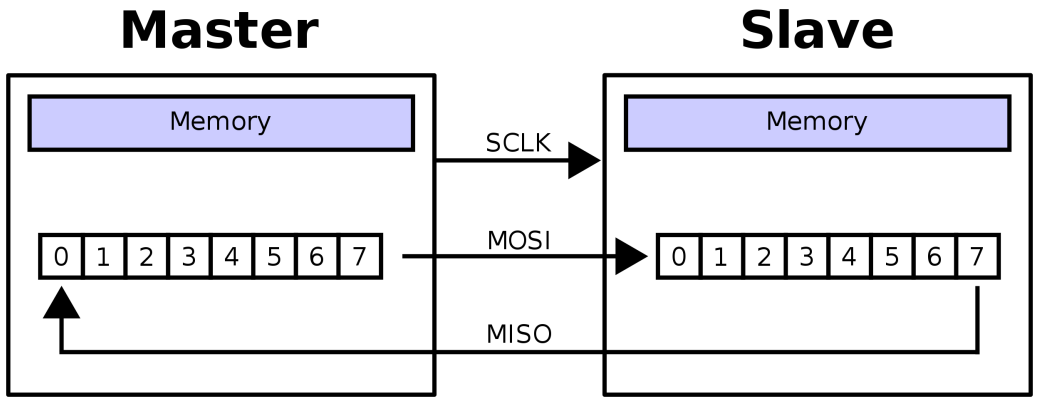
Clocks on Slave SPI

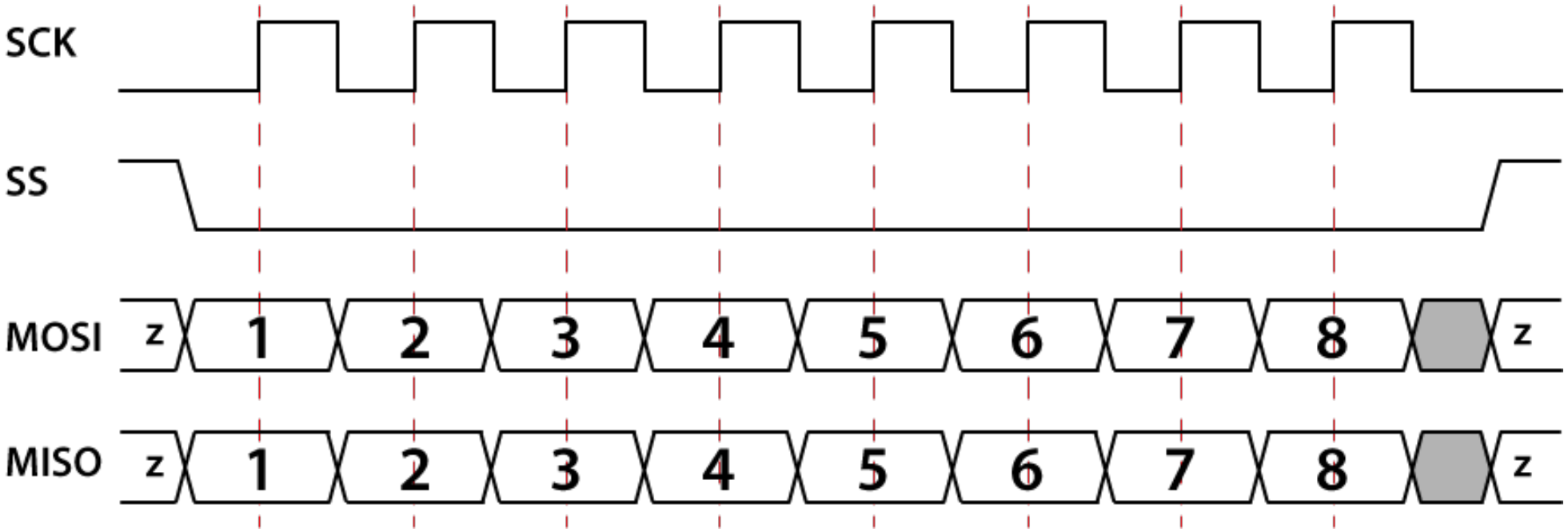




[dlnware.com]

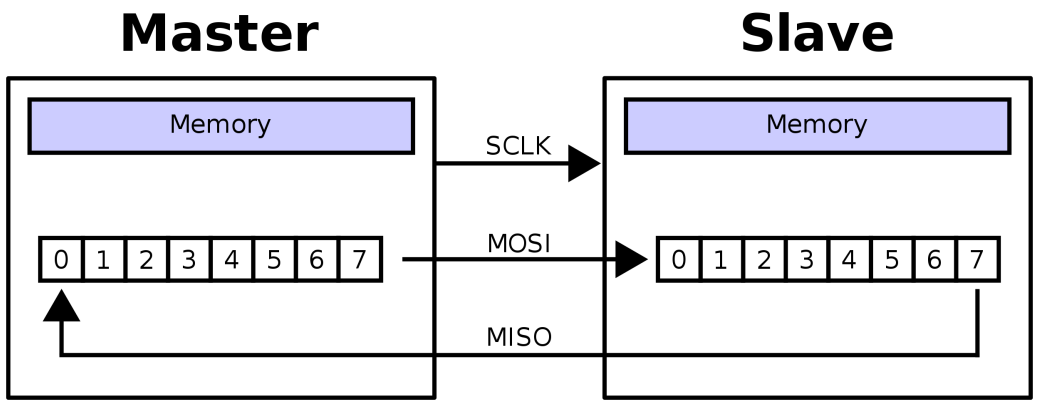
Clocks on Slave SPI

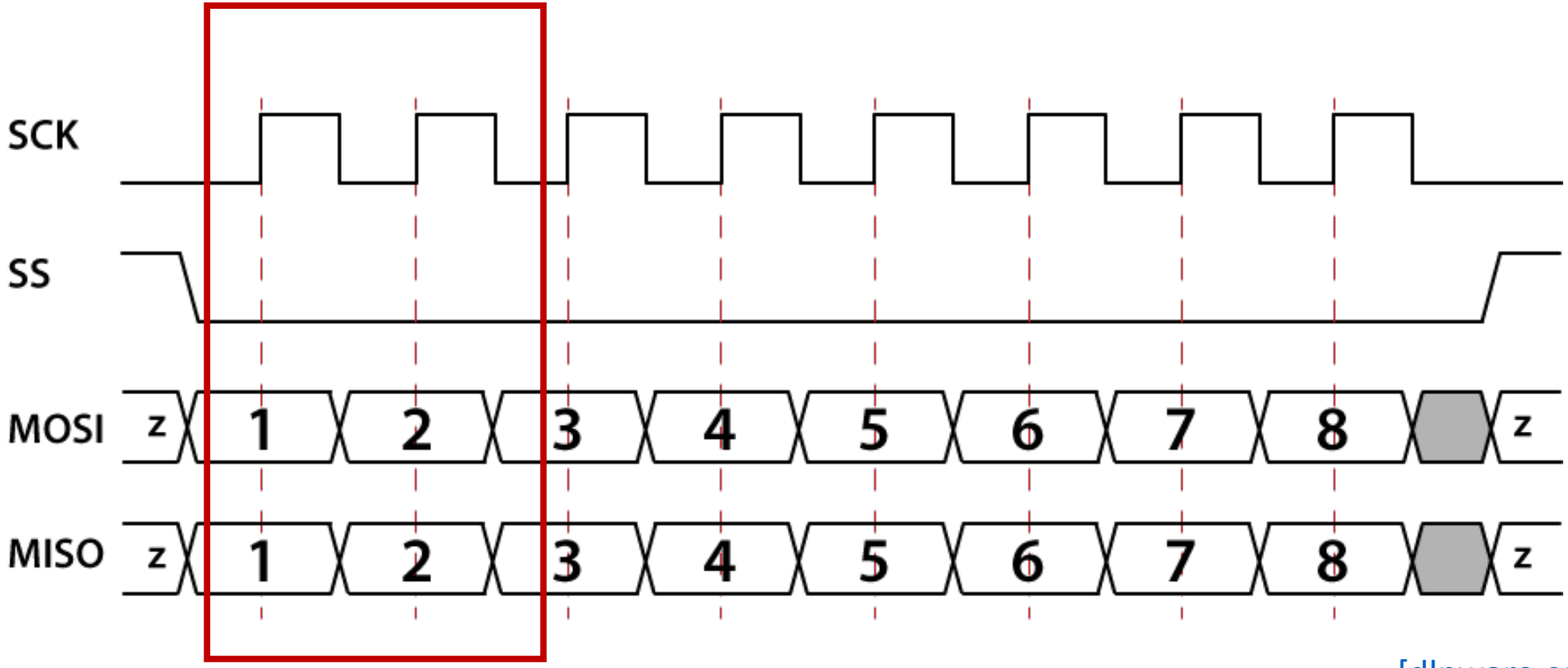




[dlnware.com]

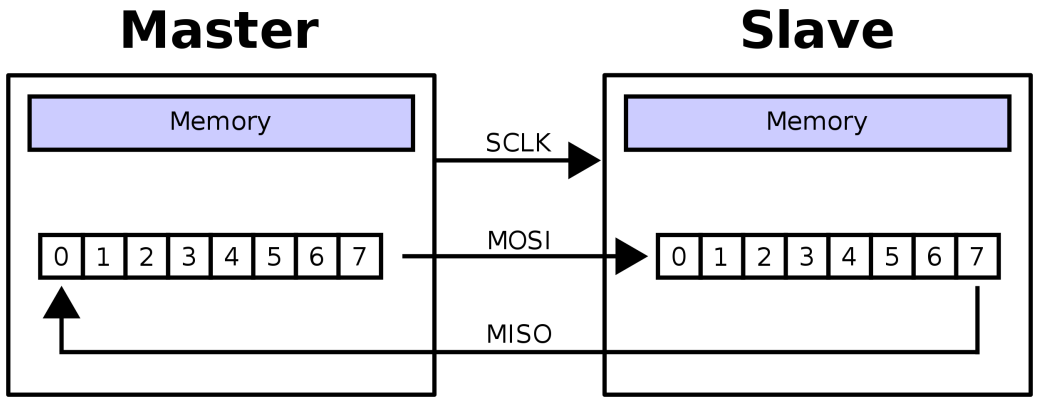
Clocks on Slave SPI



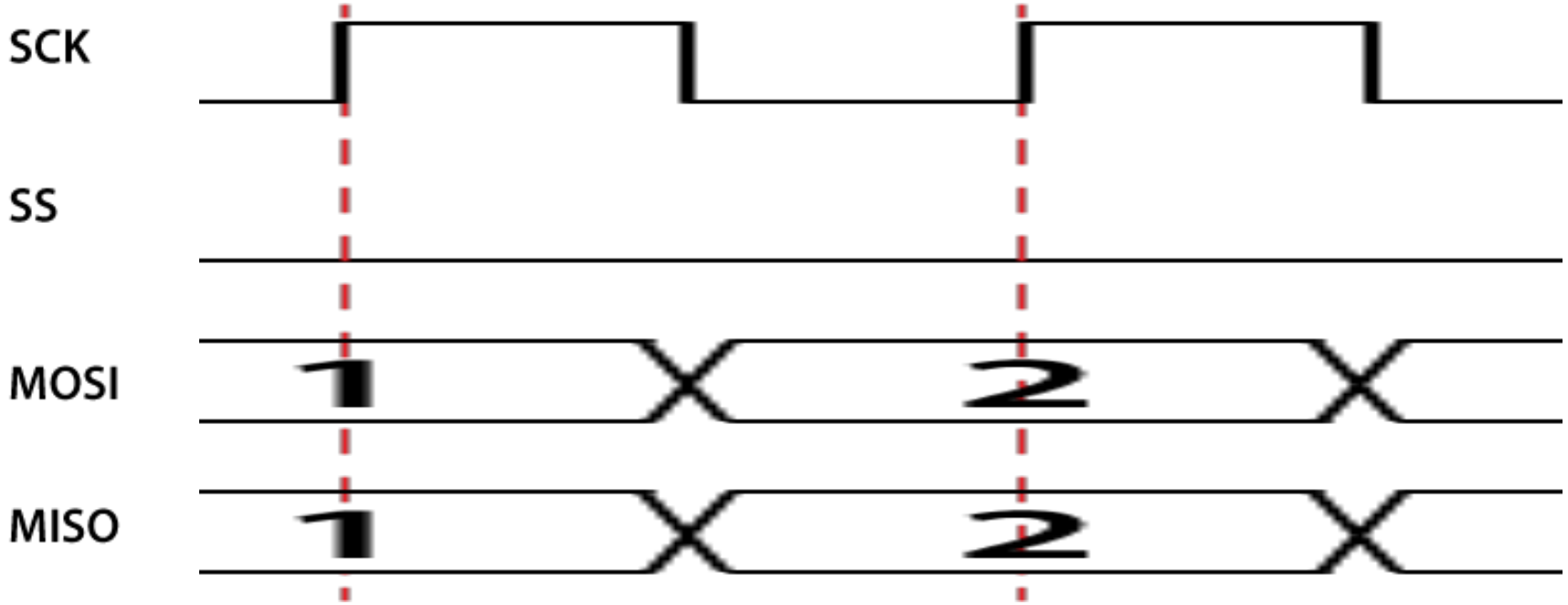


[dlnware.com]

Clocks on Slave SPI

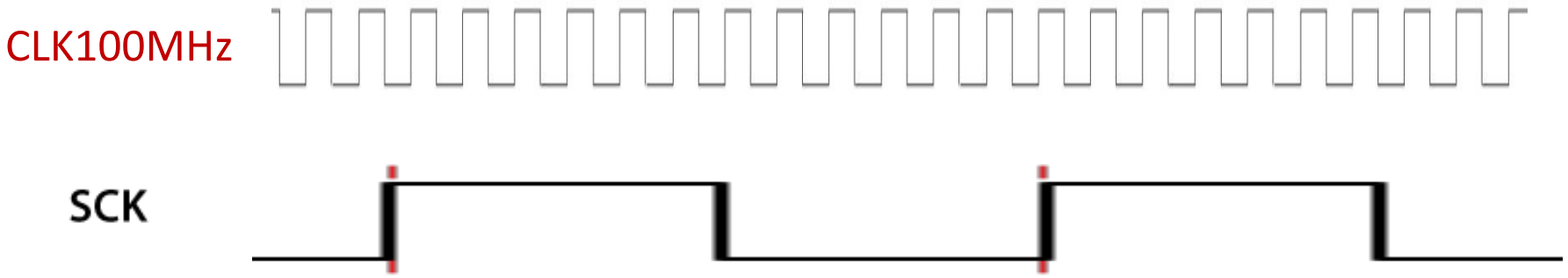


CLK100MHz

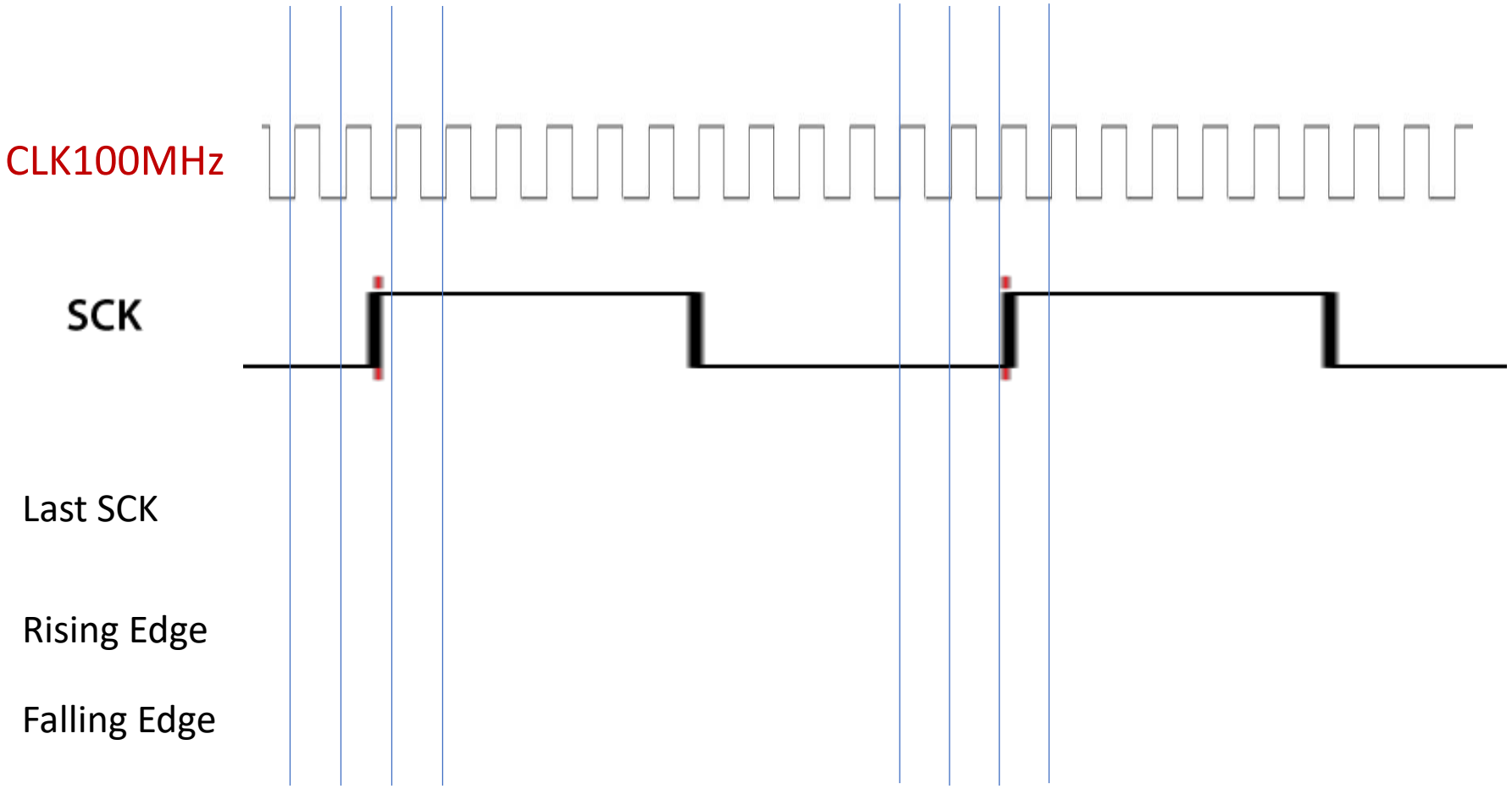


[dlnware.com]

Finding SCLK Edges

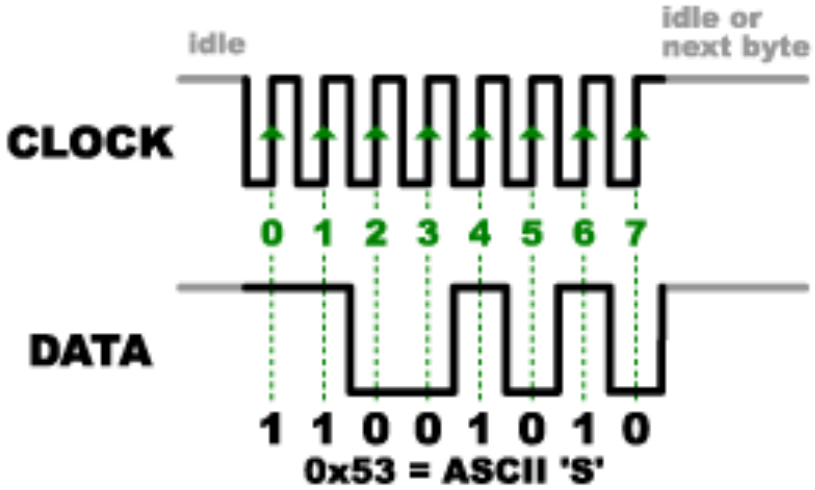


Finding SCLK Edges

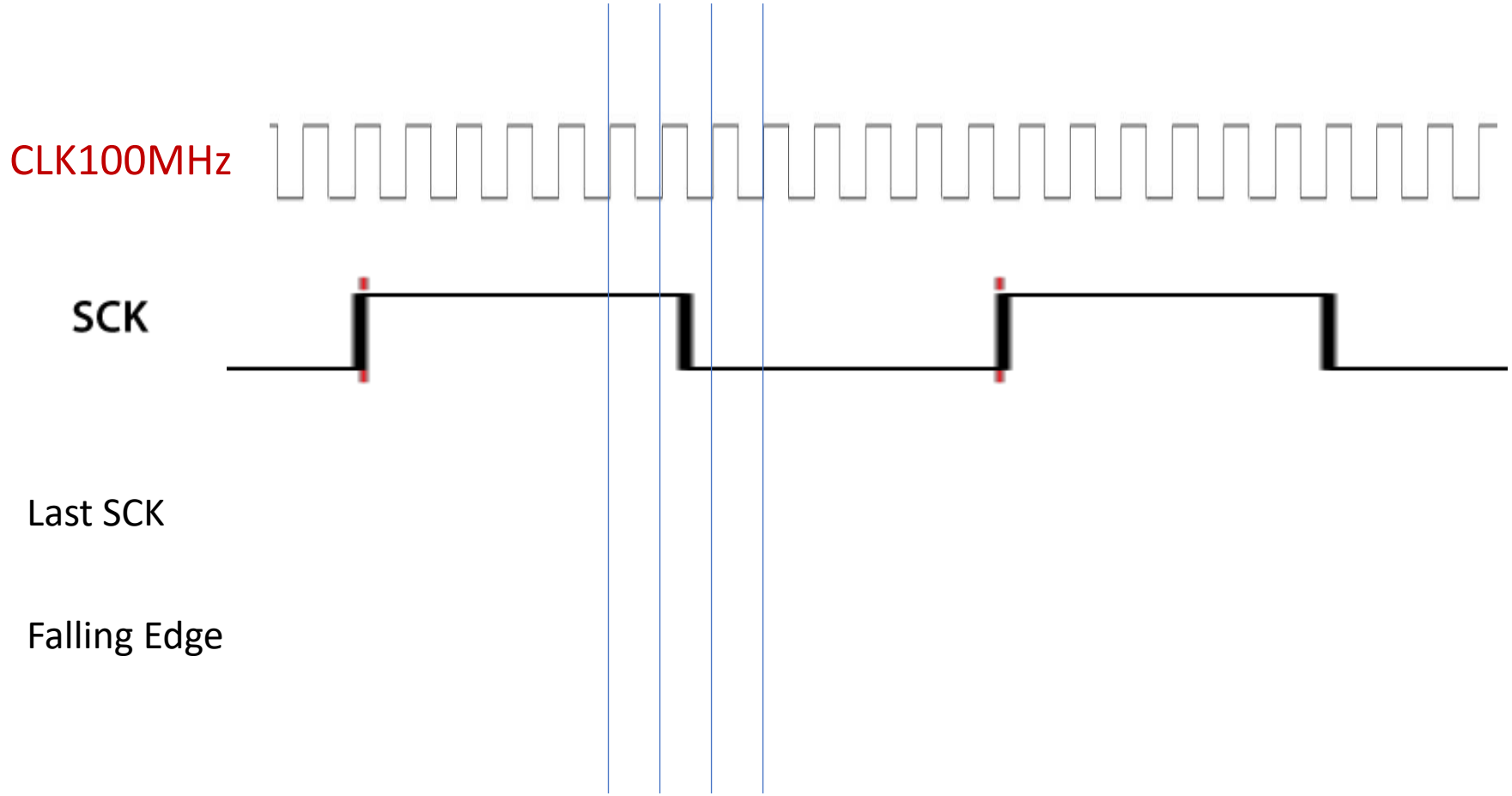


How to capture MOSI?

Not 100% right yet!



When to send MISO?

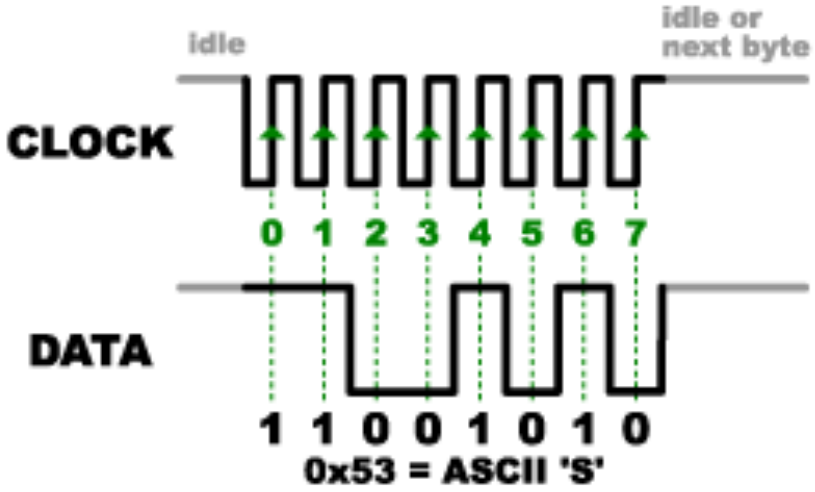


Last SCK

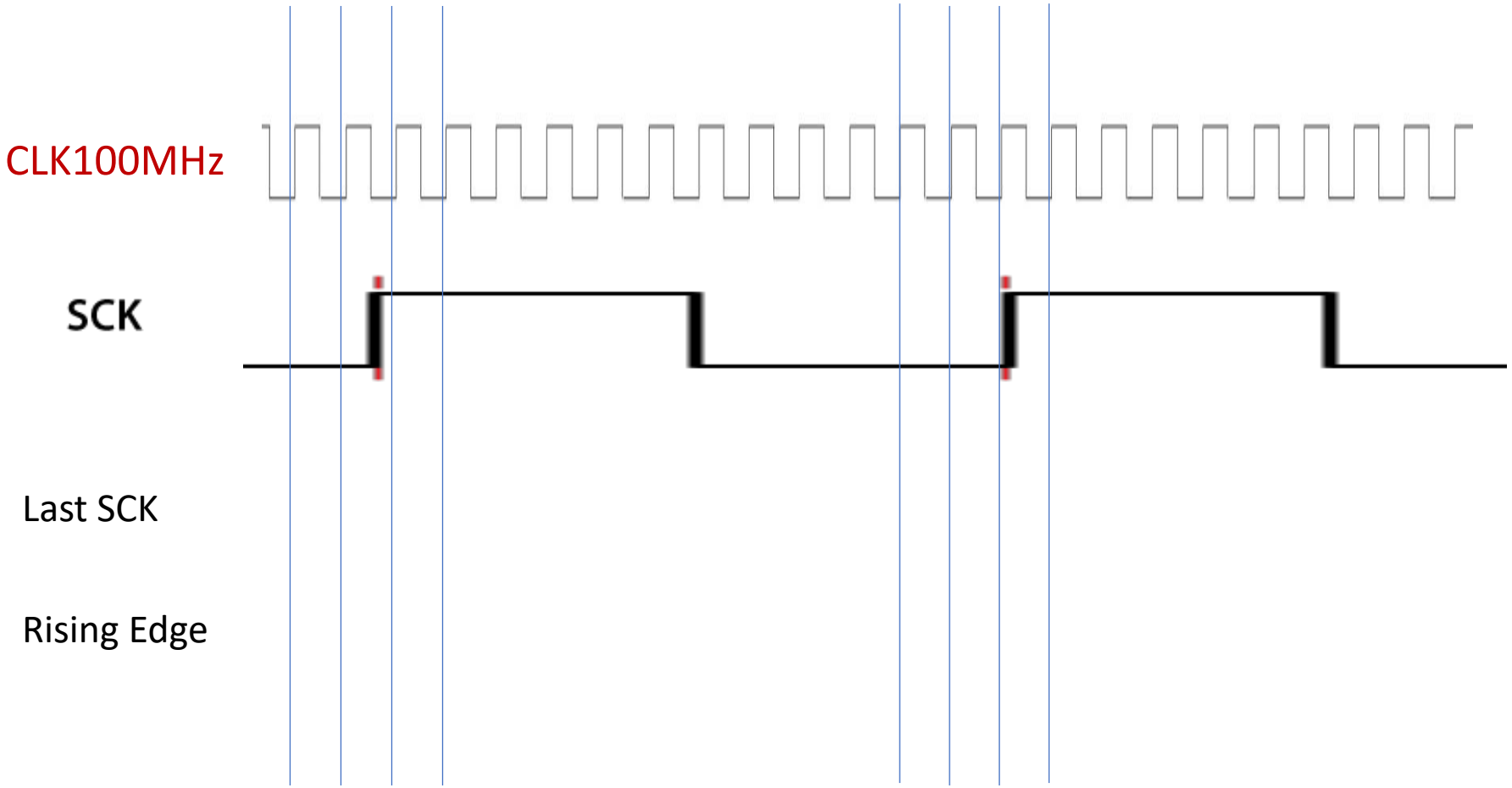
Falling Edge

How to send MISO?

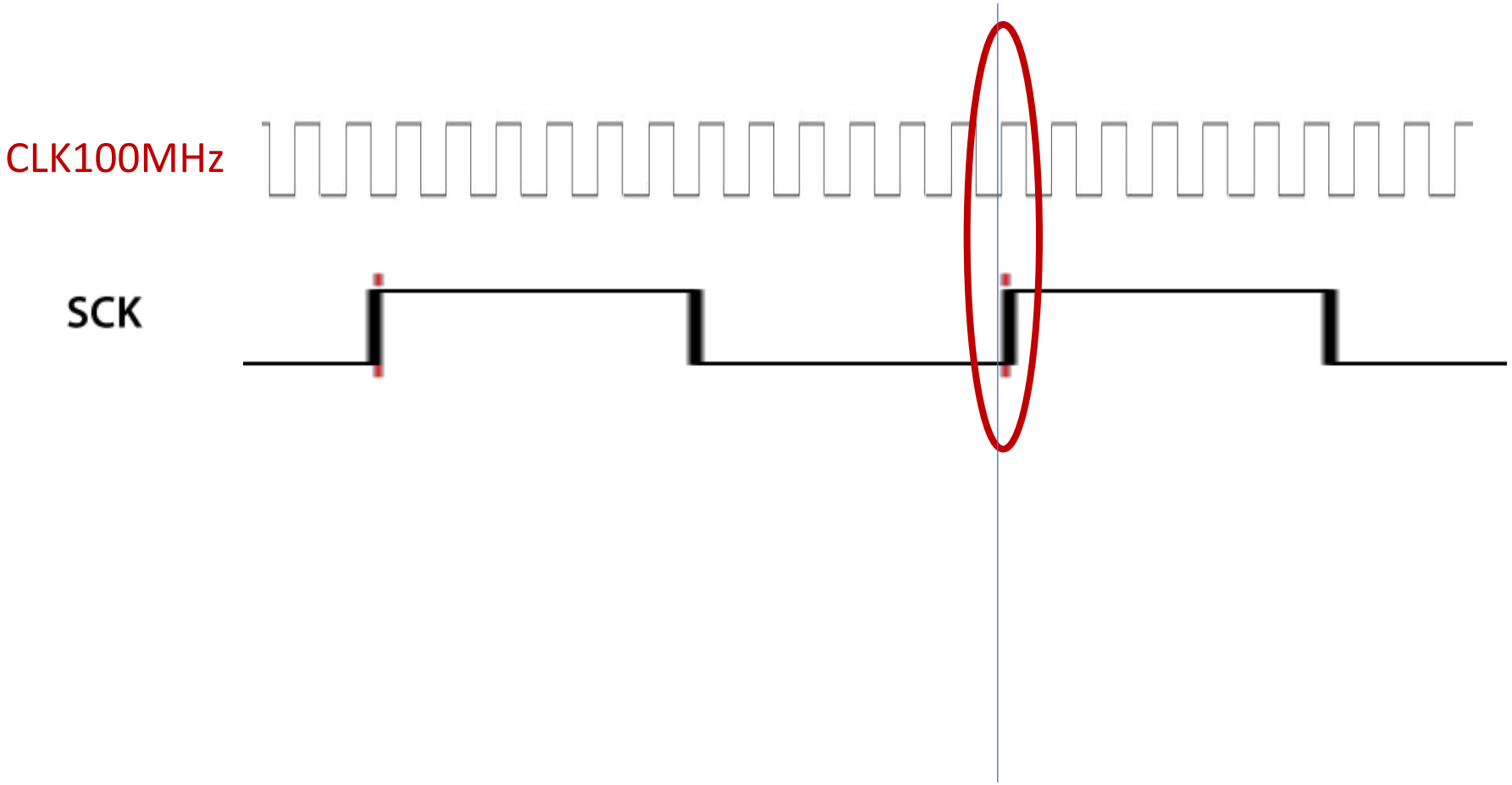
Not 100% right yet!



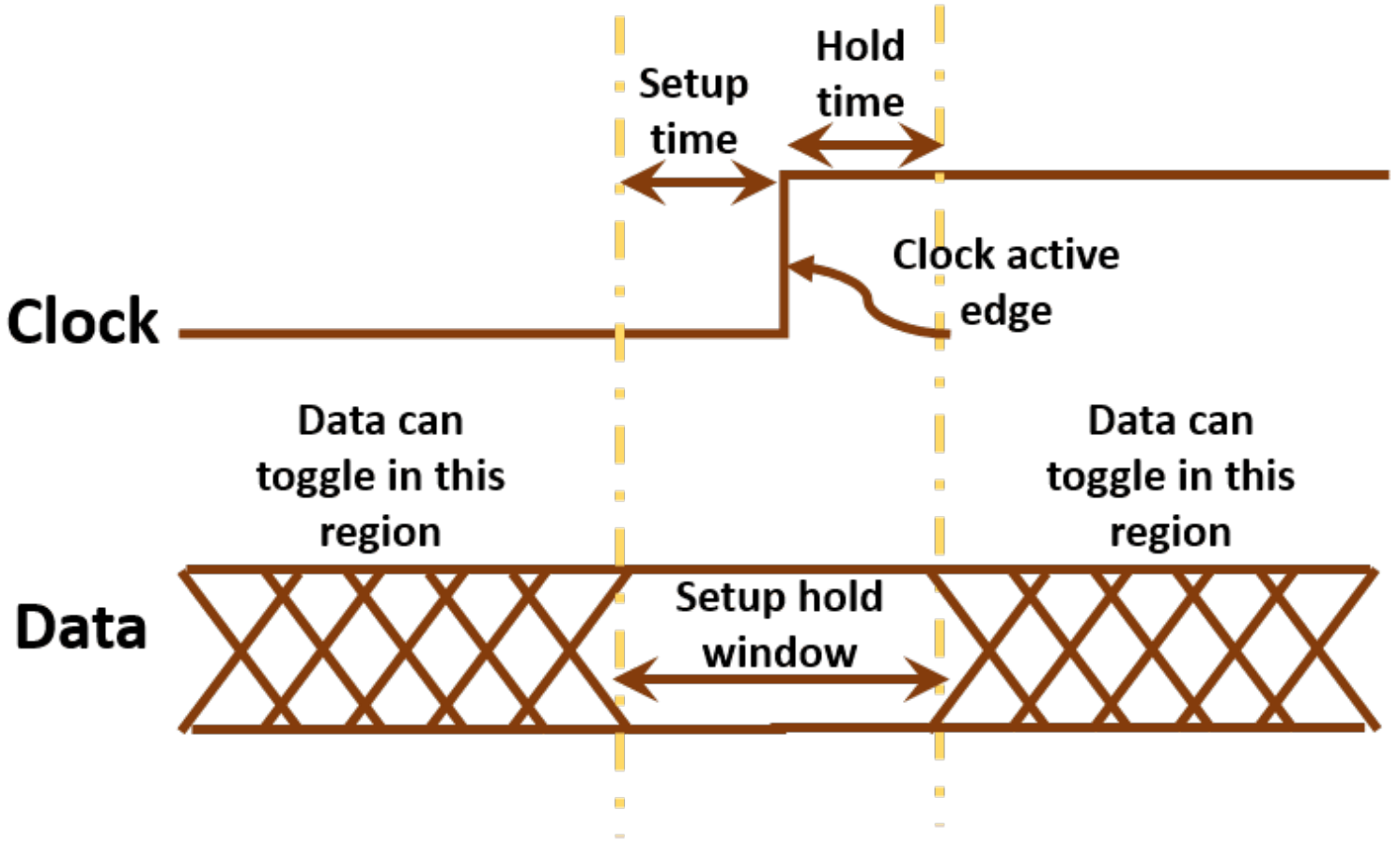
Timing Issues?



Timing Issues



Setup/Hold Time

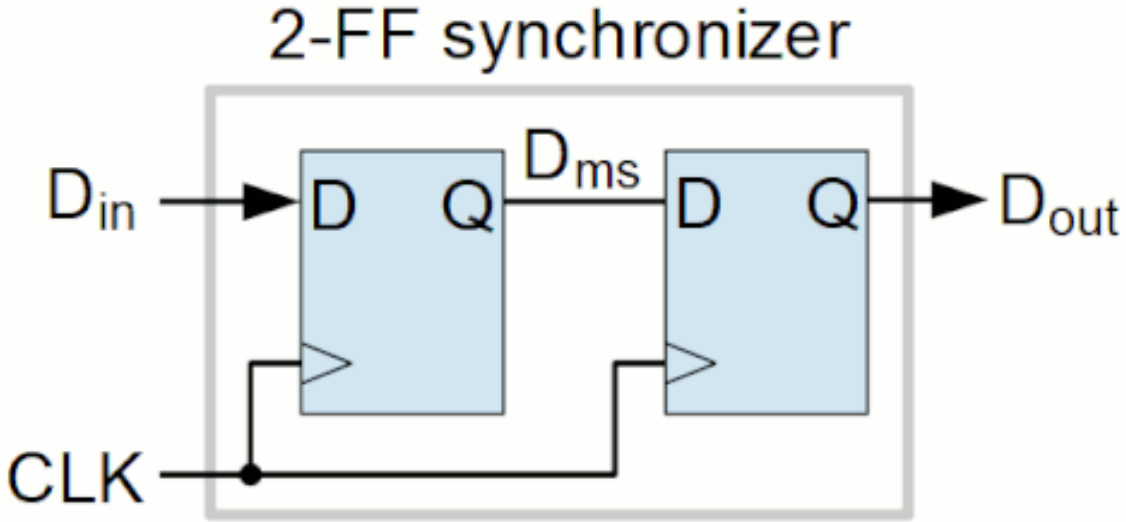


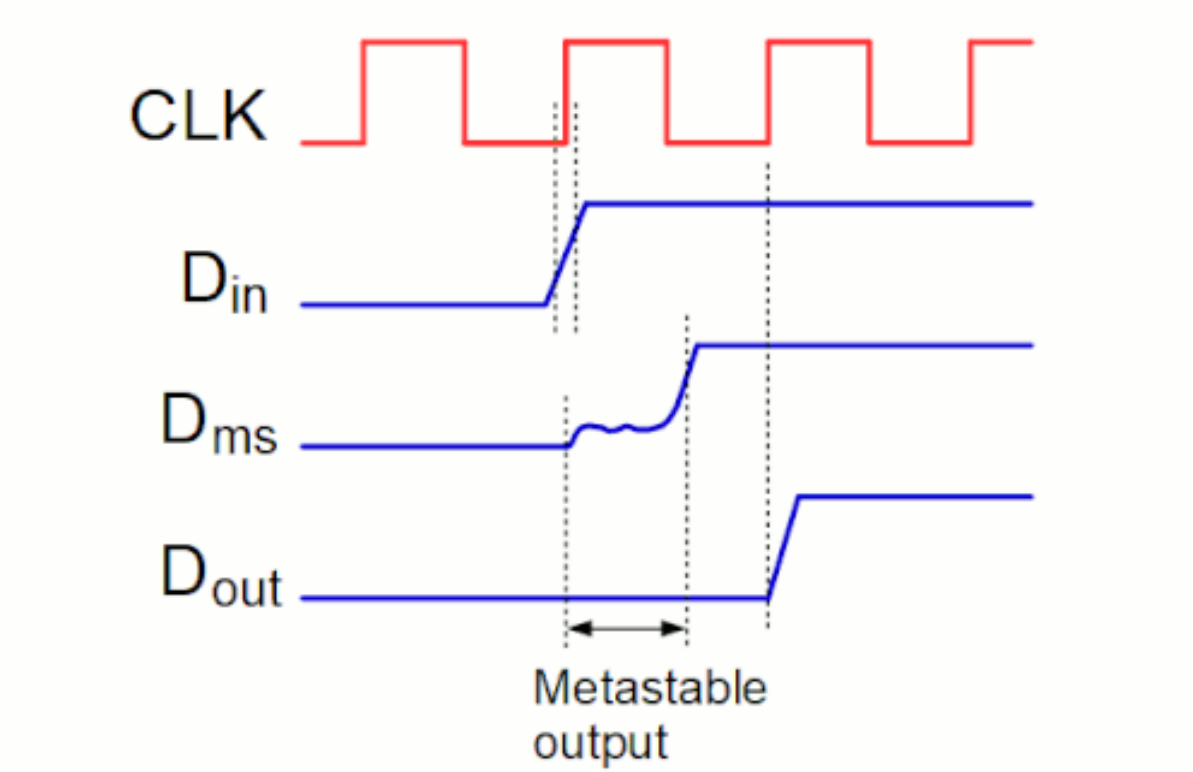
Next Time

- Synchronizers
- Tri-State Logic
- MMIO

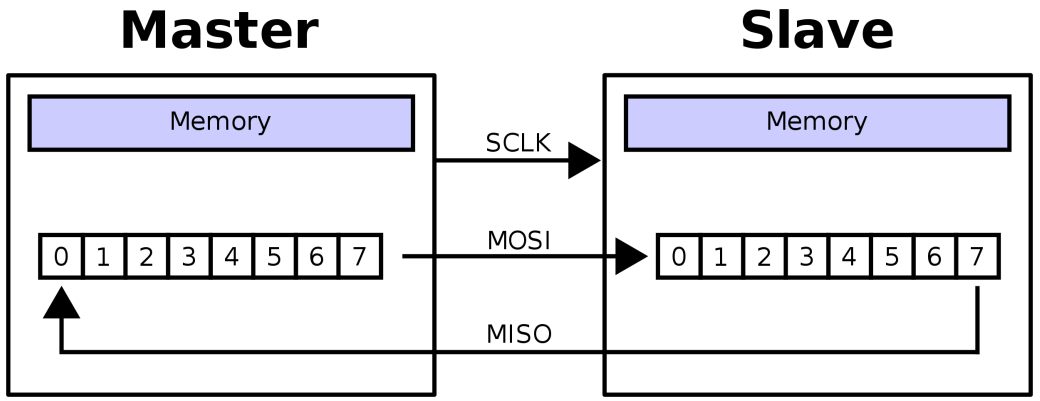
Why Synchronizers?

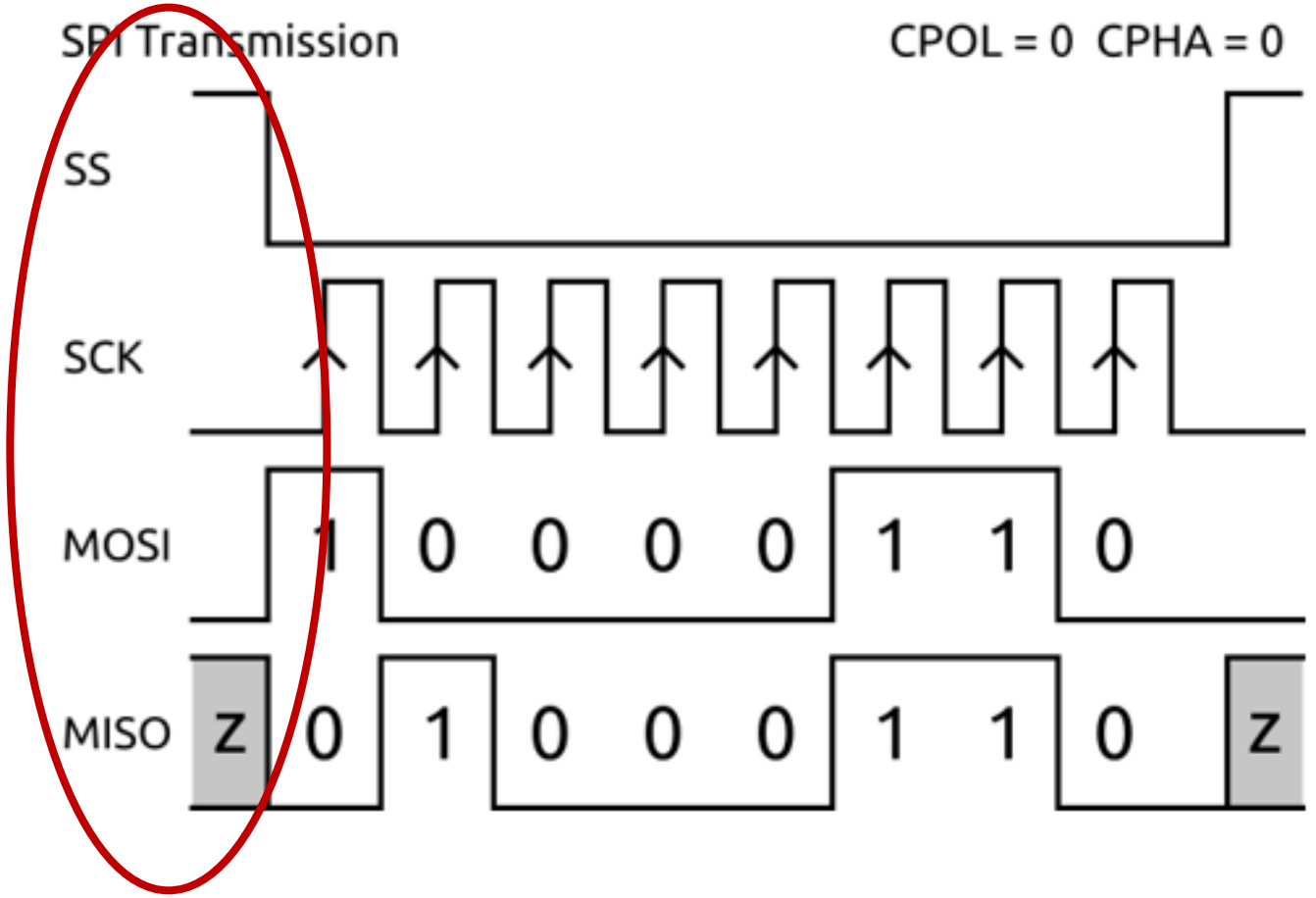
Synchronizers





What about ‘Z’?





[mathworks]

What is ‘Z’?

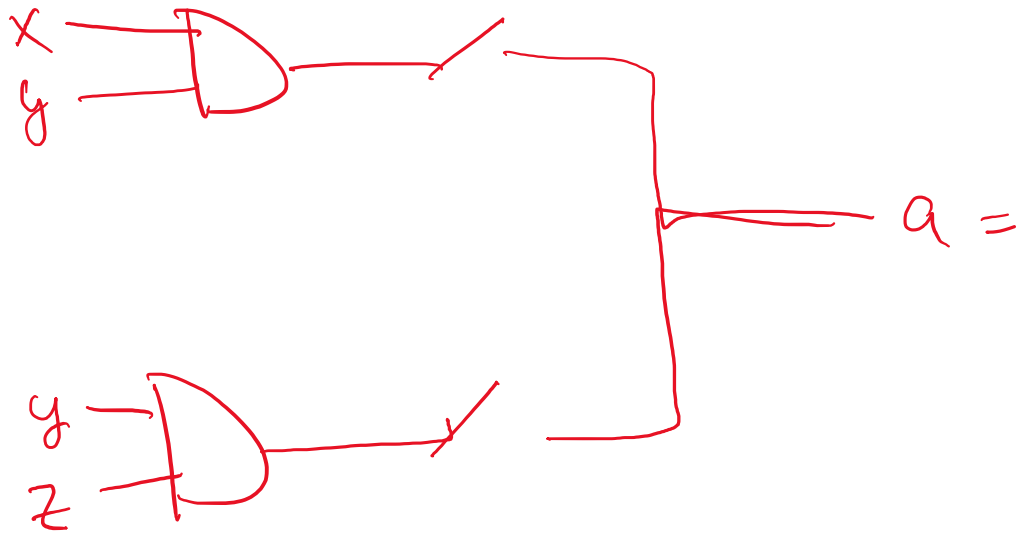
- Z: High Impedance
  - Stop driving a logical value
  - Pretend I’m not connected

- “Tri-State” signals:
  - 1: this is logical true
  - 0: this is logical false
  - X: The simulation tools don’t know if it’s 1 or 0
  - Z: this is “high impedance”

Tri-State Logic

Problems with Tri-State Logic

- What if two signals “drive” at once?



Solution: Don’t Do That!

NEVER DO THAT!